The RatCAP Front-End ASIC

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***Abstract*—We report on the design and characterization of a new ASIC for the RatCAP, a head-mounted miniature PET scanner intended for neurological and behavioral studies of an awake rat. The ASIC is composed of 32 channels, each consisting of a charge sensitive preamplifier, a 5-bit programmable gain in the pole-zero network, a 3rd order bipolar semi-Gaussian shaper (peaking time of 80 ns), and a timing and energy discriminator. The energy discriminator in each channel is used to arm the zero-crossing discriminator and can be programmed to use either a low energy threshold or an energy gating window. A 32-to-1 serial encoder is embedded to multiplex into a single output the timing information and channel address of every event. Finally, LVDS I/O were integrated on chip to minimize the digital noise on the read-out PCB. The ASIC was realized in the TSMC 0.18 μm technology, has a size of 3.3 mm $\times$ 4.5 mm and a power consumption of 117 mW. The gate length of the N-channel MOSFET input device of the charge sensitive preamplifier was increased to minimize 1/f noise. This led to a factor $\sim$ 1.5 improvement of the ENC with respect to the first version of the ASIC [1]. An ENC of 650 e-rms was measured with the APD biased at the input. In order to predict the achievable timing resolution, a model was derived to estimate the photon noise contribution to the timing resolution. Measurements were performed to validate the model, which agreed within 12%. The coincidence timing resolution between two typical LSO-APD-ASIC modules was measured using a ^{68}Ge source. Applying a threshold at 420 keV, a timing resolution of 6.7 ns FWHM was measured. An energy resolution of 18.7% FWHM at 511 keV was measured for a ^{68}Ge source.**

***Index Terms*—ASIC, CMOS, PET, PET/MR, photon noise, RatCAP, timing resolution.**

I. Introduction

BASED on our experience with previous designs, a new ASIC for the RatCAP head-mounted miniature Positron Emission Tomography (PET) scanner was realized [1]–[3]. This ASIC was specifically designed for the RatCAP project, but will also be used in the BNL PET Wrist Scanner [4], a simultaneous dual-modality PET/MRI scanner [5], and a coded aperture gamma-ray imager for homeland security applications. Significant improvements were made on this ASIC to lower the electronic and common mode noise, to add programmable gain, to lower the random input offset voltage of the timing discriminator, to add an energy gating discriminator and finally to add Low-Voltage Differential Signaling (LVDS) transceivers for communication with the Data Acquisition system (DAQ).

In Section II, the ASIC will be presented along with the design considerations. Also described is an overview of the readout system which was specifically designed for the RatCAP. Then, the measurements will be presented. Finally, the ASIC performance will be discussed, along with the validation of a model elaborated to evaluate the contribution to the timing resolution of the statistical fluctuations in the light emitted by the Lutetium Oxyorthosilicate (LSO) scintillator and the photoelectron statistics.

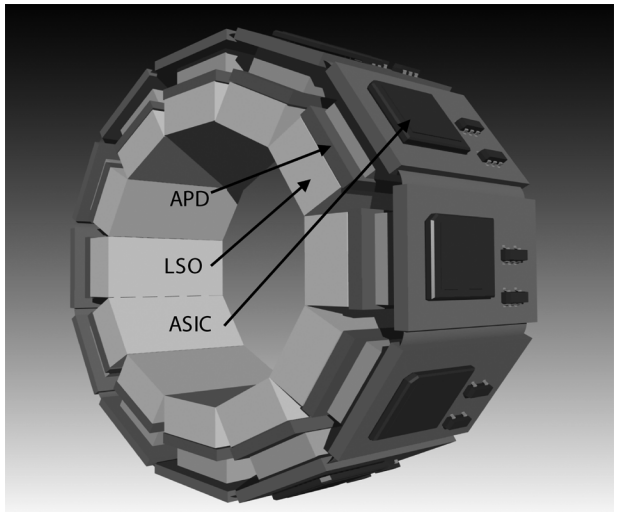

Fig. 1. Drawing of the RatCAP camera. Each detector block is composed of an LSO crystal, APD and custom ASIC.

II. The RatCAP ASIC

The RatCAP camera is composed of twelve modules of LSO and Avalanche Photodiode (APD) array coupled to the read-out ASIC, as presented in Fig. 1. The LSO array is composed of crystals of $2.2 \times 2.2 \times 5$ mm^3 coupled one to one to a 4×8 avalanche photodiode array from Hamamatsu (S8550). Each pixel of the APD has a capacitance of 10 pF and a leakage current of 1.5 nA.

The main design objectives for the front-end electronics are the following. First, it should have minimal power dissipation in

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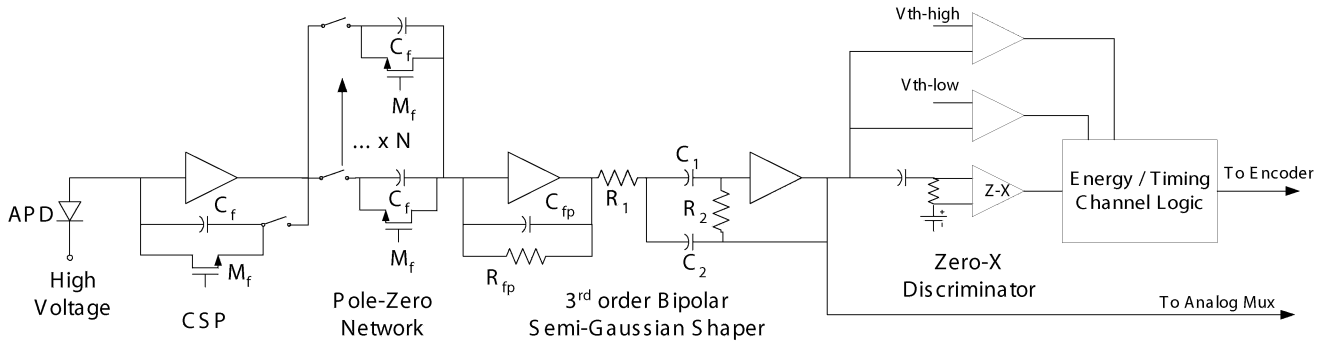

Fig. 2. Block diagram of a channel.

order not to affect the animal's behavior or affect the avalanche photodiode (APD) gain which is sensitive to temperature. Second, all the front-end electronics must be small enough to fit on the back of the detector. Third, the number of interconnections between the chips and the DAQ should be minimized in order to maximize the animal's mobility, allowing for awake animal behavioral studies. Finally, the electronics must be optimized for the detector characteristics in order to achieve the best possible timing resolution.

The mixed-signal ASIC has 32 channels. Each channel is composed of a Charge Sensitive Preamplifier (CSP), a pole-zero network with 32 programmable gain settings, a 3rd order bipolar Gaussian shaper, a zero-crossing discriminator (ZCD) used to pick off the timing information of every event and a programmable energy discriminator. Fig. 2 presents a block diagram of one channel.

A serial encoder (not shown in Fig. 2) multiplexes through a single output the digital stamp of each event occurrence and the 5-bit corresponding channel address. A 1088-bit serial programming interface (SPI) was integrated to program the gain and the energy discrimination mode of each channel as well as the analog multiplexers of the ASIC. The 100 MHz system clock of the RatCAP camera is daisy chained through the 12 ASICs. The ASIC's clock input, clock output and the serial encoder output use integrated LVDS transceivers. Two analog multiplexers, one per sixteen channels, are integrated to help in calibration and diagnosis of the analog chain. The ASIC was realized in TSMC 0.18 μm technology, has a size of 3.3 mm $\times$ 4.5 mm and has a power consumption of 117 mW. Fig. 3 presents a microphotograph of the ASIC.

A. Analog Front-End

The CSP amplifier is based on a modified telescopic cascode architecture [1]. The N-channel MOSFET input device has been optimized with respect to the technology parameters and the detector characteristics at its operating point (capacitance, leakage current and gain), using the EKV transistor model [6], to minimize the Equivalent Noise Charge (ENC) [7], [8]. The gate length was set to 0.4 μm, twice the minimum feature size, to minimize the 1/f noise contribution. With a gate width of 1760 μm and biased with 600 μA, the device is operated in weak inversion, and leads to a calculated ENC of 453 e-rms at a shaper's peaking time of 80 ns (neglecting the stray capacitance at the input). The input device has a transconductance of 13 mS and a gate capacitance of 5.8 pF. All other transistor dimensions of the CSP are optimized for minimum white series and 1/f noise contribution to the overall ENC, mainly set by the input device. The feedback capacitor is 200 fF, which gives the CSP a gain of 5 mV/fC.

The pole-zero network following the CSP is used to eliminate the non-linearity of the reset transistor M_f in the amplifier's feedback [9]. It also provides a gain N, as seen in the transfer function of the analog front-end (1), where N represents the number of pairs of capacitor C_f and reset transistor M_f in the pole-zero cancellation network:

$$H(s) = N\left(\frac{R_{fp}}{1+R_{fp}C_{fp}s}\right)\left(\frac{K\frac{\omega_p}{Q_p}s}{s^2+\frac{\omega_p}{Q_p}s+\omega_p^2}\right) \quad (1)$$

where ω_p, Q_p and K are expressed by:

$$\omega_p = \frac{1}{\sqrt{R_1R_2C_1C_2}} \quad (2)$$

$$\frac{\omega_p}{Q_p} = \frac{C_1+C_2}{R_2C_1C_2} \quad (3)$$

$$K = -\frac{R_2C_1}{R_1(C_1+C_2)}. \quad (4)$$

On a per channel basis, the factor N can be programmed between 18 to 49 in unit steps, to vary the overall front-end gain by a factor 2.7, between 21.5 and 58.5 mV/fC. A minimum of 18 $(C_f - M_f)$ pairs in the zero are required to minimize the shaper's noise contribution relative to the CSP input. This add-on was driven by the ratio of 2.5 between the pixel with the greatest charge collection to the pixel with the lowest charge collection within an LSO-APD detector module. This spread comes mainly from the light collection efficiency and APD gain variation between pixels. This leads to a wide signal dynamic range in the analog front-end which creates a considerable time dispersion in the ZCD, leading to a deterioration of the timing resolution. Also, as a single energy threshold is used for all channels, the programmable gain allows for a more uniform discrimination between the Compton scatters and the photopeak events within a detector module. It can be demonstrated that the original spread of 2.5 in the charge collection efficiency is reduced to an average of 0.033 after gain correction.

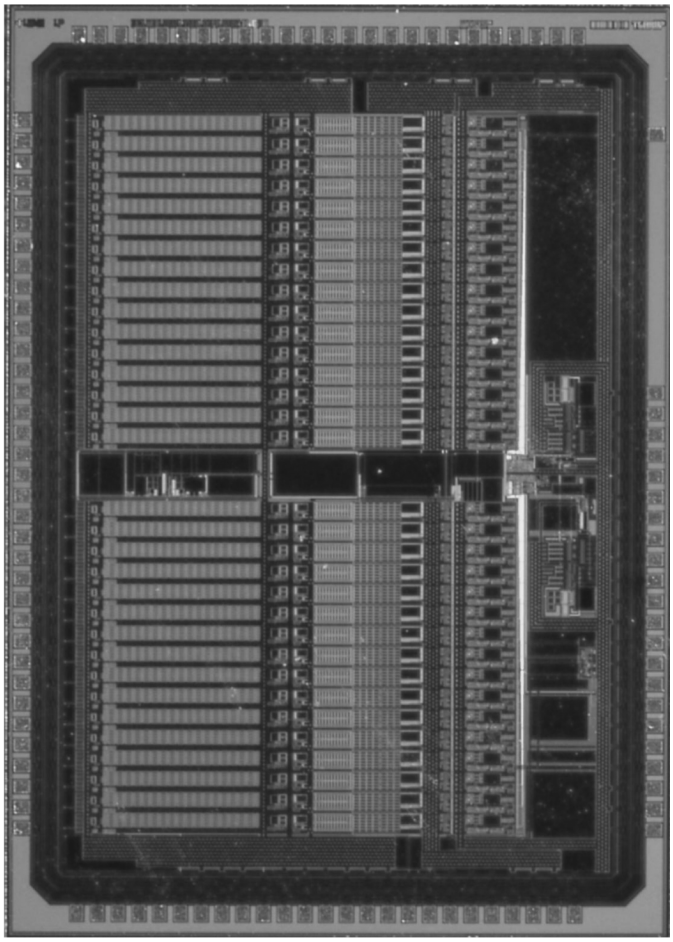

Fig. 3. Microphotograph of the RatCAP ASIC. The 32 channel ASIC was realized in TSMC 0.18 μm technology, has a size of 3.3 mm $\times$ 4.5 mm and has a power consumption of 117 mW.

The third-order bipolar semi-Gaussian shaper has a peaking time of 80 ns. It is realized in two stages: a first-order low-pass filter and a second-order bandpass filter implemented with a biquadratic architecture [10]–[12]. Both amplifiers used in the shaper are a scaled down version of the CSP amplifier, where every transistor was optimized to minimize its electronic noise contribution.

B. Timing Resolution and Photon Noise Model

The number of electron-hole pairs created as a function of time in the photodetector varies statistically from one event to another. This is due to the statistical nature of the process in which a scintillator emits visible light following the absorption of a gamma photon. The quantity and the time distribution of the emitted photons vary. Also, the photoelectron statistics in the APD, where there are the lowest quantity of information carriers [13], will affect the number of electron-hole pairs created from one event to another. This photon noise is non-stationary (time dependent) and directly affects the achievable timing resolution, one of the main figure of merit of the LSO-APD-ASIC detector module. A model of the photon noise is essential to predict a scintillator based system's performance and to validate the measurement results. Below, a procedure is presented to calculate the photon noise and the overall achievable timing resolution. Subsequently, this model will be validated in the Experimental Result section of this paper.

The timing resolution is the noise divided by the slope of the signal at the discrimination point. In a scintillator based system, the timing resolution can be expressed as,

$$\sigma_t(t_{zc}) = \frac{\sqrt{\sigma^2_{\text{noise-photon}}(t_{zc}) + \sigma^2_{ENC}}}{\frac{dV_{\text{out}}(t_{zc})}{dt}} \tag{5}$$

where the total noise is the sum of the electronic σ_{ENC} and time dependent photon noise $\sigma_{\text{noise-photon}}(t_{zc})$. The electronic noise can be calculated using [7], and it is presented in [1], [2] for this specific system. The slope at the discrimination point can be obtained by the convolution of the system's input signal from the LSO-APD response, with the impulse function of the system, expressed by (1) in this case. As a first order approximation, neglecting the finite rising edge of the APD-LSO response due to the total capacitance at the input and the effective input impedance of the preamplifier, the input signal is modeled by:

$$I_{\text{photon}}(t) = \frac{N}{\tau_{lso}} e^{(-t/\tau_{lso})} \tag{6}$$

where N is the total number of primary photoelectrons multiplied by the APD gain, and τ_{lso} is the LSO decay time constant.

Regarding the photon noise calculation relative to the CSP input, [14] presented the following expression:

$$\sigma^2_{\text{noise-photon}}(t) = qFM^2 \int_{-\infty}^{\infty} I_{\text{photon}}(\alpha) w^2(t-\alpha) d\alpha \tag{7}$$

with F, the excess noise factor [15], defined as:

$$F = Mk_{eff} + \left(2 - \frac{1}{M}\right)(1 - k_{eff}) \tag{8}$$

and q being the electron charge, M the APD gain, k_{eff} the effective ionization ratio, $I_{\text{photon}}(t)$ the LSO-APD photoelectron current (6) and $w(t)$ the weighting function of the analog front-end (1)[7], [16]. Note that $\sqrt{F}$ is the factor by which the statistical noise on the APD current (equal to the multiplied photocurrent plus the multiplied APD bulk dark current) exceeds that which would be expected from a noiseless multiplier on the basis of shot noise alone [17].

The 12 LSO-APD detector modules used in the RatCAP camera have an average APD gain of 46.8 and average of 5200 photoelectrons per MeV. For this APD gain and number of photoelectrons, the calculated slope at the zero-crossing of the bipolar shaper is 713 electrons per nanosecond. As previously mentioned the modeled ENC is 453 e-rms. Assuming an APD effective ionization ratio of 0.04, it leads to an excess noise factor F of 3.77 and a photon noise relative to the input of 1211 e-rms. Hence the average predicted timing resolution of the RatCAP camera is 1.8 ns rms for 511 keV gamma photons.

C. Energy and Zero-Crossing Discriminators

This mixed-signal circuit is composed of two comparators for energy discrimination, one comparator for generating a trigger on the zero-crossing of the shaper's bipolar signal, which represents the timing information of each event, and a logic block, as seen in Fig. 2. The comparators used for energy discrimination are identical and have a power consumption of 67.5 μW each. For better noise trigger immunity, internal positive feedback is used to create an hysteresis of 15 mV, which corresponds roughly to six sigma of the noise.

There are two main design criteria for the comparator used to trigger on the zero-crossing of the shaper's bipolar signal. First, the sensitivity of the comparator had to be high enough to minimize the energy dependent time walk for the desired input charge dynamic range, while keeping the power consumption to the minimum feasible. This is crucial, as the signal amplitude is not sent to the DAQ for post-processing of the time stamp and correction for the time walk. Second, the input stage of the comparator had to be designed to minimize input random offset voltage. Input random offset voltage acts like an offset on the reference baseline, varying from one channel to another due to its random nature. The effective consequence of having non-negligible random input offset voltage is that the comparator will not trigger at the zero-crossing of the bipolar signal, but either below or above the baseline, creating a considerable dispersion of the timing trigger as a function of energy. To minimize the random input offset voltage of the comparator, one has to take great care to match the threshold voltage and the drain current of the differential pair devices [18]. Those two parameters are functions of the input devices, but also of the load of the differential pair. For a MOSFET, the threshold voltage mismatch $\sigma_{\Delta VT}$ can be expressed as:

$$\sigma_{\Delta VT} = \frac{A_{VT}}{\sqrt{WL}} \tag{9}$$

where A_{VT} is the voltage threshold mismatch coefficient, which is constant for a given technology, and W and L are the transistor gate width and length. The drain current mismatch $\sigma_{\Delta Id/Id}$ for a device in weak inversion is expressed as:

$$\sigma_{\Delta Id/Id} = \frac{q\sigma_{\Delta VT}}{nkT} \tag{10}$$

where q is the electron charge, k the Boltzmann's constant, T the temperature and n the subthreshold slope factor [19]. In strong inversion, drain current mismatch $\sigma_{\Delta Id/Id}$ is expressed as:

$$\sigma^2_{\Delta Id/Id} = \frac{4\sigma^2_{\Delta VT}}{(Vgs - Vt)^2} + \sigma^2_{\Delta\beta/\beta} \tag{11}$$

with

$$\sigma^2_{\Delta\beta/\beta} \simeq \frac{A^2_{\mu}}{WL} + \frac{A^2_{Cox}}{WL} \tag{12}$$

where Vgs is the gate source voltage, Vt the threshold voltage, A_{μ} the carrier mobility mismatch coefficient and A_{Cox} the device oxide mismatch coefficient.

Fig. 4 presents the schematic of the comparator used to trigger on the zero-crossing of the shaper's bipolar signal. It is a differential amplifier used in open-loop, consisting of a differential input pair M1-M2 with diode connected MOSFET load M5-M6 which mirror the output signal to a push-pull output stage M8-M10. In order to improve matching between the differential input pair M1-M2, which directly affects the input random offset voltage through the variation of their threshold voltage, the gate length was set to eight times the minimum gate size. Diode connected transistors M5 -M6 are used to load the differential pair, as a lower impedance helps matching of the output current, hence the variation of the Vgs of M1-M2. It also has the benefit of lowering the voltage swing at the output of M1-M2, improving the propagation delay in the first stage. Again, the gate length of M5-M6 is bigger than the minimum size to improve their matching. To counter the loss of gain from the lower impedance of the load, current sources M3-M4 are added to increase the transconductance of the differential pair. The transistor M11 is used to cascode M8 to reduce the kick back, from the digital output stage M12-M13 through the gate to drain parasitic capacitance of M8, to the output of the differential pair. Hysteresis is not desired in the comparator to allow triggering at the zero-crossing of the bipolar signal. But still, immunity to noise triggering is essential. Hence, by driving the gate of transistor M17 to a logic low state, the comparator can be disabled by clamping one side of the differential output stage to the power supply rail, preventing any triggers from the shaper's baseline noise. To enable the comparator, the gate of M17 is pulled to a logic high state. When the comparator is enabled, the transistor M17 has minimal influence on the comparator's characteristics.

Each channel can be programmed independently to discriminate the signal's amplitude based on a low threshold, or to satisfy an energy gating window. In both energy gating modes, when a signal with an amplitude greater than the lower energy threshold is detected, the zero-crossing comparator is enabled by controlling the gate of M17 through some logic. When the energy gating window mode is enabled, the zero-crossing discriminator's trigger will be gated if the shaper signal's amplitude is greater than the upper energy threshold. Hence, to obtain the timing information of a detected event in the energy gating window mode, the shaper signal's amplitude has to be greater than the lower energy threshold, and lower than the upper energy threshold. In simulation, it is clear that there is enough time to enable the zero-crossing comparator, when the low energy condition is met, before the zero-crossing occurs. When the zero-crossing of the bipolar signal is detected, the comparator of Fig. 4 triggers. Following this trigger, all logics are reset, in order to be ready for the next event. As the digital part of the circuit is completely asynchronous, monostable circuits are used to ensure proper reset time.

D. Timing and Address Serial Encoder

One of the main design criteria of the RatCAP camera is to minimize the number of interconnections with the DAQ in order

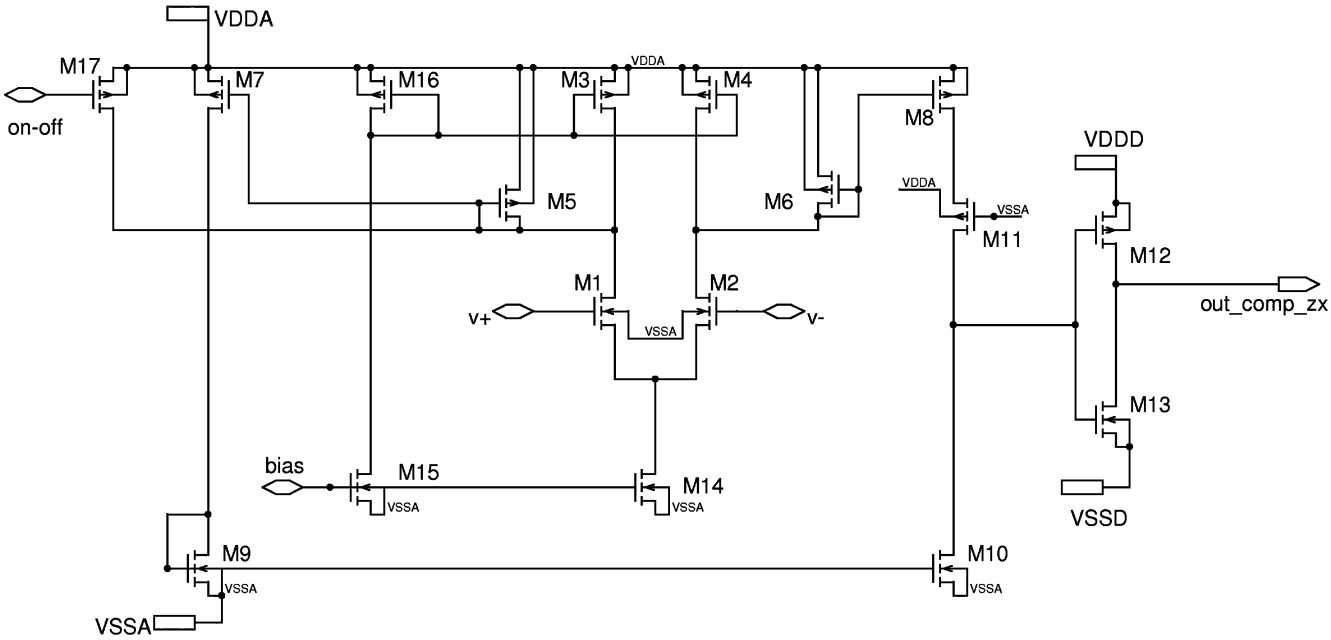

Fig. 4. Schematic of the comparator used to trigger on the zero-crossing of the shaper's bipolar signal. It is implemented using a differential amplifier in open-loop. To prevent noise triggers, the transistor M17 is used to enable the comparator only when the amplitude of the shaper's signal is greater than the low energy threshold.

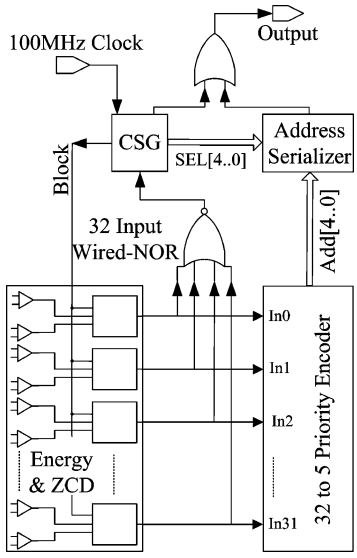

Fig. 5. Block diagram of the chip encoder. Each of the 32 channels are connected to a 32 input Wired-NOR, where the detected time of arrival of an event triggers the Control Signal Generator (CSG). The CSG will transmit the timing edge, asynchronously with respect to the 100 MHz system clock, through the single ASIC output. Each channel is also tied to a 32 to 5 priority encoder which generates the address of the channel that fired. The address is then serialized through the same output as the timing edge.

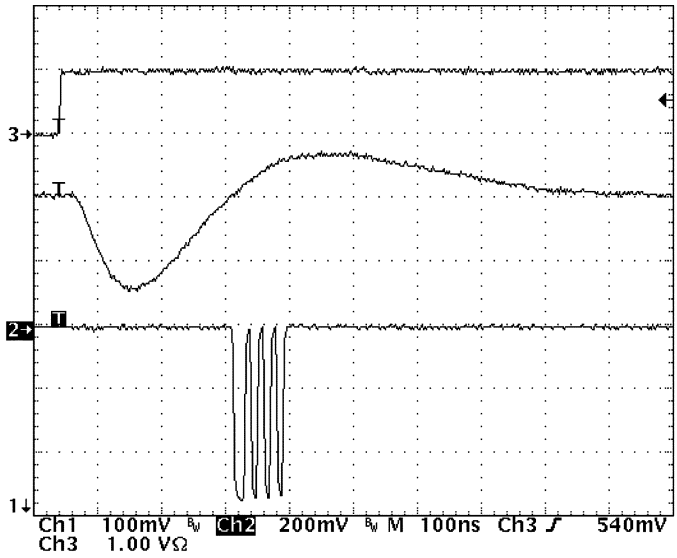

Fig. 6. Oscilloscope capture of the pulse generator trigger used to inject the charge in the ASIC (top), along with the shaper's bipolar signal (middle) and the encoder's digital output (bottom). The leading edge of the encoder's digital output represents the time of occurrence of a detected event, which is followed by the 5-bit address of the channel that fired.

to optimize the animal's mobility, which justified the implementation of a timing and address serial encoder. Fig. 5 presents a block diagram of the encoder. It consists of a wired-NOR, a Control Signal Generator (CSG), a 32-to-5 priority encoder, a serializer and an output OR gate. The encoder's output consists of a leading edge created from a wired-NOR of all 32 ZCD outputs which is asynchronous with the clock, followed by at least one clock cycle, a stop bit and then the 5 bit address of the channel that fired. Fig. 6 shows an oscilloscope capture of the encoder's output, along with the shaper's bipolar signal and the trigger of the pulse generator used to inject charge in the channel.

The 32 ZCD outputs are interconnected to the wired-NOR. Hence, when a timing trigger is generated in a channel, the wired-NOR output triggers the CSG which feeds back a blocking signal to all channels in order to prevent corruption of the chip output if another event is detected while the current event is being processed. After the last address bit has been transmitted, the CSG unblocks every channel to allow a new event to be transmitted.

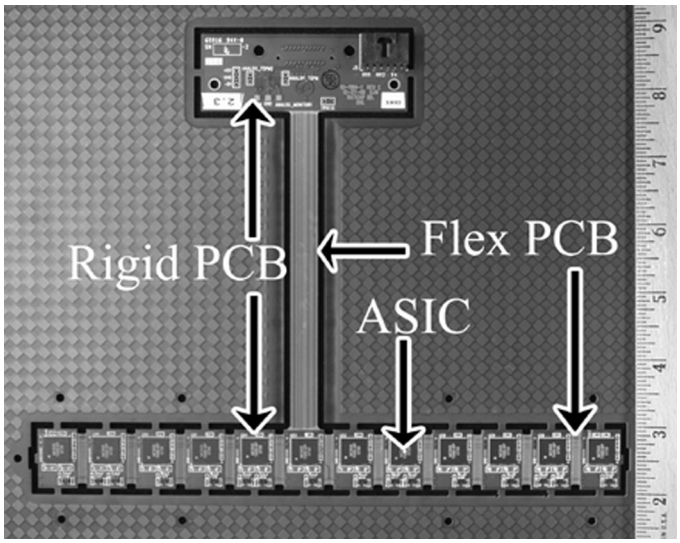

Fig. 7. Picture of the readout rigid-flex PCB of the RatCAP PET camera before being cut from the panel.

The 32 ZCD outputs are also interconnected to the 32-to-5 priority encoder. Hence, when a channel fires, the priority encoder will generate the 5 bit address which is latched in the serializer. Under the control of the CSG, the serializer will then transmit synchronously with the clock, the address to the output OR gate, starting with the LSB. In the case where more than one channel triggers the encoder before the blocking signal is broadcast, for instance in the case of a Compton scatter within the LSO scintillator array, the encoder will give priority to the higher channel address.

The synchronous part of the encoder works with a clock of 100 MHz, therefore the length of the blocking period is between 70 and 80 ns. Assuming a singles rate of about 3,125 cps per channel, a minimum efficiency of 99.3% is predictable.

E. System Readout

The Printed Circuit Board (PCB) of the RatCAP PET camera is a ten layer rigid-flex, coated with an organic solderability preservative. Fig. 7 presents a picture of the PCB. All magnetic material was removed, allowing for dual-modality PET/MR applications. Each of the twelve blocks consists of an LSO-APD array and ASIC. To minimize any common mode noise, LVDS communication protocol is being used. Each ASIC has two LVDS transmitters and one LVDS receiver embedded. The LVDS transmitter has a power consumption of 16 mW, while the receiver has a power consumption of 3.25 mW. To minimize the number of traces on the PCB, the 100 MHz system clock and the SPI are daisy chained throughout. The twelve ASICs are programmed and readout through the Timestamp and Signal Processing Module (TSPM), an FPGA-based custom DAQ system [20]. The TSPM generates a 64-bit word per detected event, which contains the absolute time stamp of the detected photon as well as the address of the channel that fired. An average 1.2 million events per second are expected for the RatCAP, and the maximum rate capability of the DAQ is 80 MB per second. The data is acquired in list mode, and coincidence matching is performed offline using a software which also performs a timing offset calibration to correct for time dispersions between the 384 channels [21].

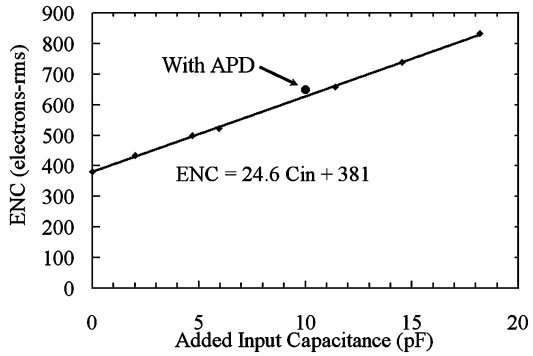

Fig. 8. ENC as a function of input capacitance. The marker represents the measured ENC of 650 e-rms with the APD biased at a gain of 45.

III. Experimental Results

The ASIC has been thoroughly tested and is fully functional. Out of 35 packaged ASICs of 32 channels each, a total of 4 channels were not responding, leading to a yield of 99.6%.

A. Equivalent Noise Charge

The ENC of the front-end was measured for various capacitances at the input, and is reported in Fig. 8. The ENC was also measured with the Hamamatsu APD S8550 biased at a high voltage of 353 V to obtain the noise figure at the nominal operating gain of 45. An ENC of 650 e-rms was measured. The measurements were performed with the ASIC on a test PCB with the 100 MHz LVDS system clock, the serial programming interface and the digital output of the ASIC operational in order to obtain realistic results. By extrapolating the curve to the abscissa, a total capacitance at the input of 15.5 pF is deduced, where the gate capacitance of the input NMOS of the CSP is 5.8 pF, the input pad is 500 fF and the feedback capacitor of the CSP is 200 fF. Hence a stray capacitance at the input of about 9 pF is estimated. By comparison, the calculated ENC taking into account the stray capacitance and the APD noise figure, considering solely the noise of the input device and neglecting the noise from the shaper and any digital activity, leads to a value of 645 e-rms, which is in good agreement with the measurement. This calculated ENC of 645 e-rms differs from the 453 e-rms presented in Section II-A, as the stray capacitance was originally neglected.

To evaluate the contribution from the digital activities in the ASIC and on the PCB to the ENC, it was measured again but this time with only the analog front-end enabled. A negligible improvement was noticed, meaning that the digital activities had negligible effect. It is expected that the digital noise may have a greater impact on the rigid-flex PCB designed for the RatCAP camera caused by the higher density of digital traces near the via interconnecting the detector anodes to the ASIC input, due to the limited real estate.

B. Energy Resolution

Energy spectra for all channels can be obtained simultaneously in the system by taking the derivative of the measured

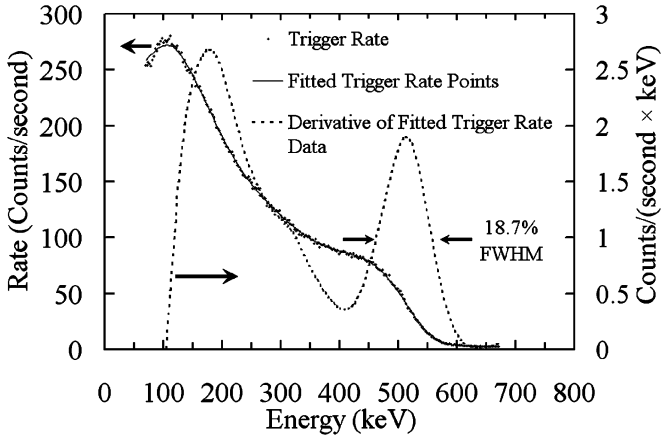

Fig. 9. Energy spectra of an LSO-APD-ASIC detector module using a $^{68}\mathrm{Ge}$ source. An energy resolution of 18.7% ($\Delta E = 95.5\,\mathrm{keV}$) FWHM is measured.

output trigger rate as a function of the energy threshold. For example, Fig. 9 displays such a spectrum, where the trigger rate data, the fit of the trigger rate data and its derivative as a function of the energy threshold is displayed. An energy resolution of 18.7% ($\Delta E = 95.5$ keV) FWHM is measured for a typical channel connected to an APD-LSO detector using a $^{68}\mathrm{Ge}$ source.

C. Timing Jitter and Time Walk

The electronic timing jitter and time walk were measured. A voltage pulse from a Tektronix AFG3251 function generator is fed to the test input of the ASIC, where an integrated analog multiplexer allows one to choose which channel to stimulate. A Tektronix TDS6804B oscilloscope is used to histogram the leading edge of the ASIC's encoder output relative to the function generator trigger signal. The mean and the distribution width of the histogram represent the time walk and the timing jitter, respectively, for a given amount of charge injected in the channel. The measurements were performed without a load at the input, having solely the stray capacitance of 9 pF. Fig. 10 presents the mean, standard deviation, minimum and maximum timing jitter of all the channels measured. Considering the ratio of 2.5 between the photopeak position of the pixel with the greatest charge output to the pixel with the lowest charge output, and assuming an average energy resolution of 20% FWHM, the effective dynamic range is from 5.4 fC to 22.8 fC. Hence a maximum electronic jitter of 1.8 ns rms is expected. An average time walk of 0.7 ns is measured for a shaper signal amplitude between 310 mV and 520 mV, the effective dynamic range where all photopeaks will be aligned using the programmable gain of each channel.

D. Timing Resolution and Scintillator Photon Noise Model Validation

The photon noise model was validated for two arbitrary channels. Table I presents the measured number of photoelectrons, APD gain and ENC for both channel.

To validate this model, the timing resolution due to the photon noise $\sigma_{t-\mathrm{photon}}(t_{zc})$ was measured indirectly by subtracting the

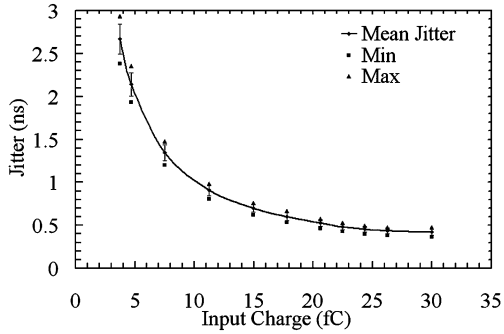

Fig. 10. Electronic timing jitter at the encoder's output. The error bars represent the rms deviation of all the channels measured. Also plotted, the minimum and maximum measured jitter as a function of input charge.

TABLE I
MEASURED CHARACTERISTICS OF THE TWO CHANNELS USED IN THE TIMING RESOLUTION MODEL. THE NUMBER OF PHOTOELECTRONS, APD GAIN AND EQUIVALENT NOISE CHARGE ARE PRESENTED

	Channel 1	Channel 2
Number of P-E/MeV	5990	4220
APD Gain	45	53.5
ENC (e-rms)	648	664

TABLE II
COMPARISON OF THE MODEL WITH THE MEASUREMENTS OF THE TIMING RESOLUTION FOR THE TWO CHANNELS UNDER TEST. THE TOTAL TIMING RESOLUTION, ALONG WITH THE CONTRIBUTION FROM THE ELECTRONIC NOISE AND PHOTON NOISE ARE PRESENTED. (ALL RESULTS IN NS RMS).

	Channel 1			Channel 2		
	Measured	Model	Error	Measured	Model	Error
σ_{T-ENC}	0.9 ns	0.8 ns	11%	0.9 ns	1.0 ns	-11%
$\sigma_{T-LSO}(t_{zc})$	1.7 ns	1.6 ns	5.9%	1.7 ns	1.9 ns	-12%
$\sigma_{T-total}(t_{zc})$	1.9 ns	1.8 ns	5.3%	2.0 ns	2.2 ns	-10%

timing resolution due to the electronic noise $\sigma_{t-\mathrm{electronic}}$ from the overall measured timing resolution $\sigma_t(t_{zc})$:

$$\sigma^2_{t-\mathrm{photon}}(t_{zc}) = \sigma^2_t(t_{zc}) - \sigma^2_{t-\mathrm{electronic}}. \tag{13}$$

It is important to note that the timing resolution contribution from the electronic noise has to be measured for an ideal LSO-APD input signal, and not for the delta response of the system. This can be achieved by applying the following voltage pulse using a waveform generator to an injection capacitor C_{inj} tied to the front-end input:

$$V(t) = \frac{Q_{in}}{C_{inj}} U(t-t_0)\left(1 - e^{-(t-t_0)/\tau_{lso}}\right) \tag{14}$$

where Q_{in} is the total amount of charge injected. The total timing resolution $\sigma_t(t_{zc})$ of the LSO-APD-ASIC module was measured with an energy window of 15.5 keV centered on the 511 keV photopeak, in coincidence with a BaF_2-PMT detector.

Table II presents the calculated and measured timing resolution, along with the respective contribution from the electronic noise and photon noise.

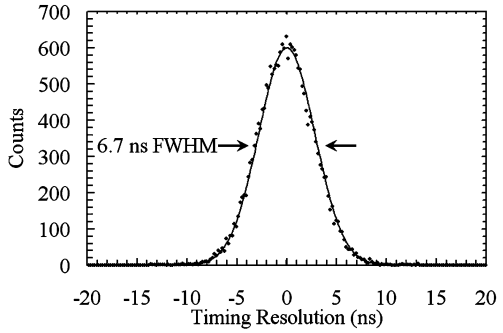

Fig. 11. Coincidence timing resolution between two APD-LSO-ASIC detector modules. Energy threshold was set at 420 keV.

The first conclusion is that the model is valid, predicting within 12% the photon noise contribution. Second, it is interesting to notice that the zero-crossing discriminator's timing resolution is dominated by the photon noise. This is due to the fact that the timing measurement is achieved at the zero-crossing of the shaper's bipolar signal roughly 280 ns after the first photon being emitted by the scintillator, hence suffering from a large integration of the photons fluctuation and photoelectron statistics from one event to another.

The coincidence timing resolution between the two previous LSO-APD-ASIC detector modules was measured for a ^{68}Ge source, with an energy threshold set at 420 keV. Fig. 11 shows the spectrum, where a coincidence timing resolution of 6.7 ns FWHM was obtained from the fit, which is also in good agreement with the model. The measured coincidence timing resolution, one of the main figures of merit of the LSO-APD-ASIC detector module, is comparable to performance achieved with other LSO-APD based-PET systems in the field [22], [23].

IV. Conclusion

The ASIC for the RatCAP small animal PET camera was presented. The ASIC is fully functional and is currently used in the BNL RatCAP project, dual-modality PET/MRI, Wrist scanner apparatus, and finally in a coded-aperture gamma-ray imager for Homeland Security applications. The implementation of this new ASIC was justified by the improved performance where the ENC was lowered significantly, programmable gain was embedded to compensate for the light collection and APD gain variations, the timing and energy discriminator were improved, and finally LVDS transceivers were integrated to minimize the digital noise on the readout PCB. A future revision of the ASIC is being discussed, where the timing discriminator would be replaced by an architecture in which the photon noise would be minimized. Also, global and trimming digital to analog converters would be integrated to have independent energy thresholds in each channel.

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