Front-End Electronics for the RatCAP Mobile Animal PET Scanner

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***Abstract*—We report on the development of the front-end electronics for rat conscious animal positron emission tomography (RatCAP), a portable and miniature positron emission tomography scanner. The application-specific integrated circuit (ASIC) is realized in a complementary metal–oxide–semiconductor 0.18 μm technology and is composed of 32 channels of charge sensitive preamplifier, third-order semi-Gaussian bipolar shaper, timing discriminator with independent channel adjustable threshold, and a 32-line address serial encoder to minimize the number of interconnections between the camera and the data acquisition system. Each chip has a maximum power dissipation of 125 mW. A mathematical model of the timing resolution as a function of the noise and slope at the discrimination point as well as the photoelectron statistics was developed and validated. So far, three ASIC prototypes implementing part of the electronics were sent to fabrication. Results from the characterization of the first two prototypes are presented and discussed.**

***Index Terms*—Avalanche photodiodes (APDs), complementary metal–oxide–semiconductor (CMOS), mixed analog-digital integrated circuits, positron emission tomography, rat conscious animal positron emission tomography (RatCAP).**

I. Introduction

A TEAM at the Brookhaven National Laboratory is currently working on the realization of the rat conscious animal positron emission tomography (RatCAP) scanner. The RatCAP is a head-mounted miniature positron emission tomography (PET) scanner intended to perform brain imaging and behaviorial studies of awake rats [1]. The requirement of mobility imposes significant limitations on the size, weight, power dissipation, and data communication with the scanner, requiring new approaches to detectors, electronics, and image reconstruction.

In this paper, we report on the development of the front-end electronics for the RatCAP. The main design objectives for the front-end electronics are the following. First, the application-specific integrated circuit (ASIC) should have minimal power dissipation in order not to affect the animal's behavior or change the avalanche photodiode (APD) gain which is sensitive to temperature. Second, all the front-end electronics must fit on the back of the detector. Third, the number of interconnections between the chips and the data collection module (DCM) should be minimized in order to prevent the degradation of the camera's mobility. Finally, the electronics must be optimized for the detector characteristics in order to achieve the best possible timing resolution.

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II. The RatCAP Front-End Electronics

A. The RatCAP System

The RatCAP system is composed of a 384 channel camera with a communication and power management module, an absolute time and address generator module, and a versa module eurocard (VME)-based acquisition system. The detectors are based on Hamamatsu 4×8 APD arrays (S8550) coupled to lutetium oxyorthosilicate (LSO) scintillators of $2 \times 2 \times 5$ mm^3. These detectors have a measured light output of 4500 photoelectrons per MeV. The camera is made of 12 detector blocks, each having a 32-channel front-end ASIC mounted on the back. The main purpose of the ASIC is to provide the position and the timing information of every detected event. Also, on the back of each detector block, there is a 1.8 V voltage regulator and circuitry for independent high voltage trimming of each APD array. In order to minimize the number of interconnections, an on-chip encoder sends the timing information as well as the detector channel address through one output.

The communication module converts 0–1.8 V signals (camera side) to low-voltage differential signal standard I/O data. There is also an analog driver for channel monitoring and calibration with an oscilloscope, as well as a 100 MHz clock generator for the ASIC's digital circuit.

On the receiving end, the proposed DCM will be made of a field-programmable gate array based time-to-digital converter, which will detect the timing edge with a subnanosecond resolution. A 64 bit word will be generated for each event, where 43 bits are for an absolute time stamp, 13 bits are for the detector channel and ASIC addresses (flexibility to go to 256 blocks), 7 bits are for a timer-counter to check for memory overflow, and the last 3 bits are for event type classification. The data are read out with a VME-based data acquisition system and sent to a Linux-based computer system for storage and analysis.

B. The RatCAP ASIC

Fig. 1 presents a block scheme of the RatCAP ASIC. Every channel contains a charge sensitive preamplifier (CSP), a

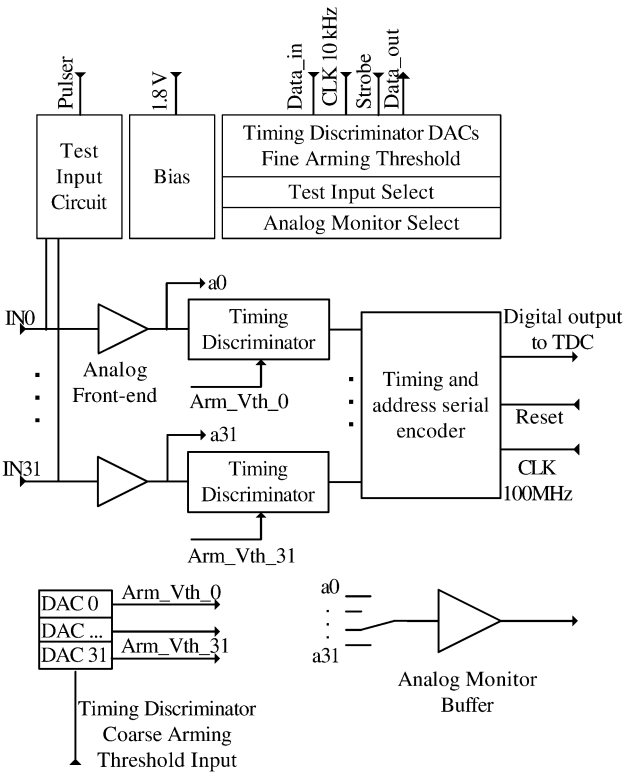

Fig. 1. Block diagram of the RatCAP front-end ASIC.

pole-zero cancellation network, a third-order bipolar Gaussian shaper [2], and a timing discriminator with programmable arming threshold. The ASIC also includes a 32 line timing and address serial encoder used to send the address of the detector channel, following the asynchronous timing edge. Finally, circuitry for diagnostic and calibration is built-in on chip. The chip is realized in a 0.18 μm, single poly, six metal, salicide complementary metal–oxide–semiconductor (CMOS) process from Taiwan Semiconductor Manufacturing Company.

The CSP is based on the telescopic cascode architecture, with an added current source $(M2)$ into the input device to allow greater transconductance, as shown in Fig. 2. As a shaper implementing a short peaking time is used where white series noise dominate, an n-channel MOS (NMOS) was selected for the input device of the CSP for its greater noise performance compared to a p-channel MOS (PMOS) [3]. Also, knowing the limited power budget, the NMOS allows a greater transconductance than the PMOS. Fig. 3 shows a schematic of the analog front-end section. The feedback capacitor C_f (300 fF) sets the gain of the CSP to 3.3 mV/fC. The reset transistor M_f, is an NMOS as the leakage current of the APD flows into the CSP, which collects holes from the anode of the APD connected to the input. The gate of the reset transistor is biased using a voltage reference independent of process variations. The power dissipation is 1.3 mW.

The parameters of the NMOS input device have been established by mathematical simulations using *MathCAD* and the EKV transistor model. They have been optimized with respect to the technology parameters and the detector characteristics at its operating point (capacitance, leakage current, and gain) to minimize the equivalent noise charge (ENC)

$$\mathrm{ENC} = \sqrt{\mathrm{ENC}_f^2 + \mathrm{ENC}_p^2 + \mathrm{ENC}_s^2} \tag{1}$$

$$\mathrm{ENC}_f^2 = C_{in}^2 \frac{K_{Fn}}{C_{ox} W L} \pi A_f \tag{2}$$

$$\mathrm{ENC}_p^2 = \frac{2kTA_p t_p}{R_{eq}} \tag{3}$$

$$\mathrm{ENC}_s^2 = \frac{2kTA_s C_{in}^2}{t_p} \left(\frac{\gamma}{g_{m_N}} + R_P \right) \tag{4}$$

with

$$R_{eq} = \frac{R_{p1}}{N^2} \left\| \frac{2kT}{I_{\mathrm{leak}} M} \right\| \frac{1}{\eta g_{m_{FB}}} \tag{5}$$

where ENC_f is the flicker noise, ENC_p the parallel noise, ENC_s the series noise, C_{in} the total capacitance at the input, K_{Fn} the NMOS flicker noise coefficient, C_{ox} the gate oxide capacitance per unit of area, W and L the width and length of the input NMOS, A_x the form factors of the shaper [4], k the Boltzmann's constant, T the temperature in Kelvin, t_p the shaper peaking time, γ the coefficient of thermal noise for the input MOS field-effect transistor, gm_N the source transconductance of the input NMOS, R_P the parasitic resistance in series with each transistor electrode, R_{p1} the first pole feedback resistance of the shaper, N the charge gain factor of the pole-zero compensation network, I_{leak} the APD leakage current, M the APD gain, η a coefficient that depends on the region of operation, and gm_{FB} the transconductance of the reset transistor. Mathematical simulations predict an ENC of about 726 electrons rms at 70 ns peaking time. Table I summarizes the characteristics of the CSP, where the calculated inversion coefficient, simulated transconductance, gate capacitance and gain-bandwidth, and measured input noise voltage (e_n) and rise time are presented. A similar CSP prototype, using 5 mW, has been developed. Further design details and evaluation of both CSPs can be found in a companion paper [5].

A pole-zero cancellation network is used to compensate the reset transistor nonlinearity [6]. It is also used to reduce the parallel noise contribution of the following stage by providing a charge gain equal to N.

The third-order bipolar Gaussian shaper is realized in two stages: a first-order low-pass filter and a second-order bandpass filter implemented with the biquadratic architecture [2], [7], [8]. Both amplifiers used in the shaper are a scaled version of the CSP amplifier, where every transistor was optimized to minimize its electronic noise contribution. The analog chain has a gain of 15.15 mV/fC and the shaper power consumption is 600 μW. Table II presents the values of the passive components integrated in the analog front-end section shown in Fig. 3.

An investigation is under way to establish the optimum timing discriminator, the shape, and the peaking time of the shaper signal to optimize the timing resolution. An initial study was realized taking into account an estimation of the series noise, the photoelectron statistics, and the slope of the shaper signal as a function of the peaking time. With a zero-crossing discriminator (ZCD), a peaking time of 70 ns was found to lead to a minimum

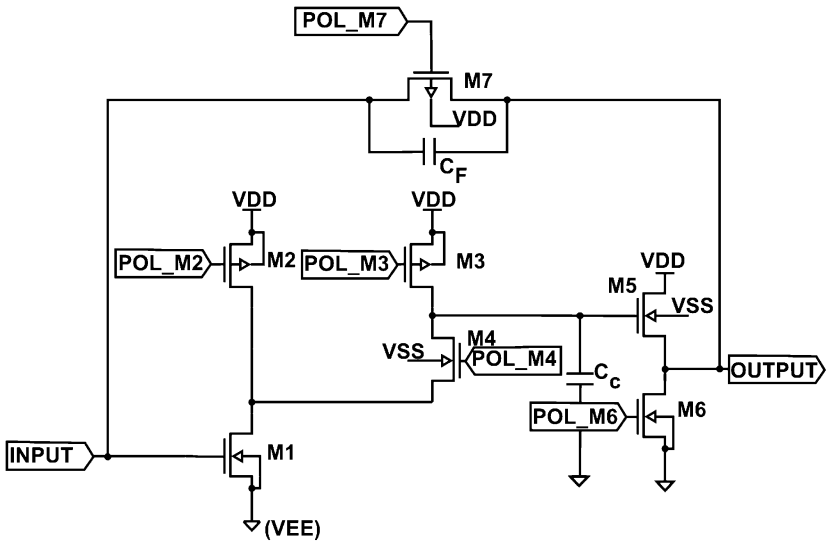

Fig. 2. CSP architecture.

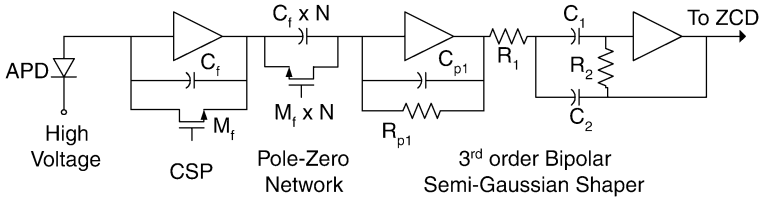

Fig. 3. Analog front-end.

TABLE I
RATCAP CSP CHARACTERISTICS

Input NMOS device	
Inversion coefficient	0.35
Transconductance	13.5 mS
Gate capacitance	1.5 pF
CSP	
Input noise voltage (e_n)	0.9 nV / $Hz^{1/2}$
Rise time (C_{in} = 12pF)	17.2 ns
Gain-Bandwidth	255 MHz

TABLE II
VALUES OF PASSIVE COMPONENTS OF THE ANALOG FRONT-END

C_f	300 fF	C_{p1}	1.241 pF	R_2	97.5 kΩ
M_f (W/L)	0.3 μm / 1 μm	R_{p1}	95.7 kΩ	C_1	7.125 pF
N	18	R_1	22.9 kΩ	C_2	0.75 pF

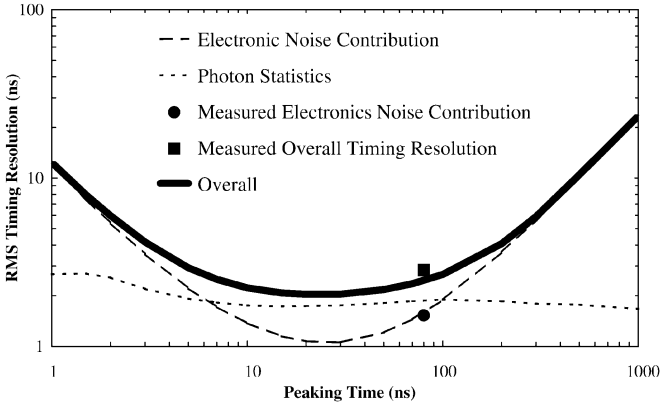

Fig. 4. Calculated and measured timing resolution of the analog front-end using a zero-crossing discriminator. A light output of 2300 photoelectrons and an APD gain of 50 was used.

timing resolution of 700 ps rms. Hence the first shaper prototype was implemented with a 70 ns peaking time. After measuring the ENC of the CSP on the first ASIC prototype, and using the measured impulse response of the CSP and the third-order bipolar Gaussian shaper, an estimated timing resolution of about 2.5 ns rms was obtained at 70 ns peaking time. Fig. 4 presents the mathematical simulation results, with the photoelectron statistics and electronic noise contributions, as well as the measured timing resolution.

As stated previously, a study is currently in progress to determine the type of timing discriminator to be used. So far, the proposed solution is a ZCD based on two comparators. One is used for arming the ZCD by triggering on the leading edge of signals at a threshold set independently for each channel using 5 bit digital-to-analog converter (DAC). A coarse threshold will be provided externally in order to set the ZCD minimum threshold in the valley between the Compton events and the photopeak of the weakest gain channel. The 5 bit DAC minimal step is then established to allow the threshold to span the range from the weakest to the strongest gain channel. The other comparator is used to find the baseline crossing of the bipolar signal, which actually represents the timing information of every event. In order to calibrate the camera and set every channel's threshold to compensate for gain variation from the APD and the front-end electronics, the count rate as a function of the channel threshold will be measured. The 5 bit DACs are set for every channel by a shift

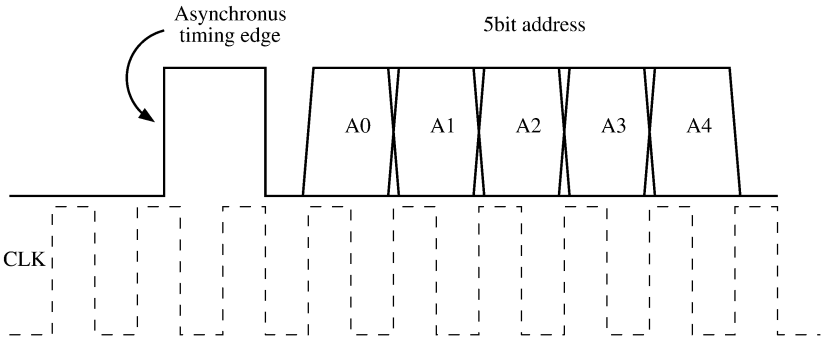

Fig. 5. Output of the serial encoder.

register loaded serially, where the shift registers of the 12 chips are daisy chained.

In order to minimize the number of external connections, a 32 line address serial encoder is included on-chip. When an event is detected by a channel, the timing discriminator triggers a wired-OR connected to the logic encoder block. At this moment the address is encoded as a 5 bit binary number. This number is latched into a register on the falling edge of the clock, one full clock cycle after the timing edge coming from the wired-OR. The asynchronous timing edge and the latched 5 bit address are transmitted on a single line, serially. Fig. 5 illustrates the serial encoder output signal. Conflict between two or more simultaneous triggers is resolved by priority encoding, neglecting lower valued addresses. The encoder uses a 100 MHz clock and has negligible power consumption. The impact of serializing the 32 channel outputs, assuming a maximum rate of 30 000 cps per channel, leads in the worst case to a minimum efficiency of 93.3%. Measurement of the singles rate for a detector block is 100 000 cps, or 3125 cps per channel. Hence, this would lead to a minimum efficiency of 99.3% in the worst case.

Also, included on chip, is an analog multiplexer that allows the monitoring of the shaper signal through an on-chip analog driver.

Thus far, three ASICs were sent for fabrication through the Canadian Microelectronics Corporation (CMC). The first one (ICFSHLNA) has test structures and two CSPs with external bias needed. The second one (ICFSHB01) has 32 channels of CSP and shaper with on-chip bias network. The third one (ICFSHB02), which has not been tested yet, has 16 channels of CSP, shaper, ZCD with external common threshold setting, and serial encoder. The final chip is designed to have a maximum power budget of 125 mW (1.5 W for the entire camera) and the estimated final size is 1.7×4.2 mm^2.

III. Experimental Results

A. ICFSHLNA Measurements

The CSP electronic characterization, timing resolution, and energy resolution were performed on the ICFSHLNA chip. The ENC of the CSP, connected to Hamamatsu's APD S8550 and a custom made $CR^2 - RC^2$ shaper, has been measured as a function of the peaking time and is presented in Fig. 6. The minimum ENC is 1116 electrons at 100 ns. The measured ENC has been fitted using (1). An input-referred noise voltage (e_n) of 0.9 nV/$\sqrt{\text{Hz}}$ and input-referred noise current (i_n) of 0.181 pA/$\sqrt{\text{Hz}}$ were deducted.

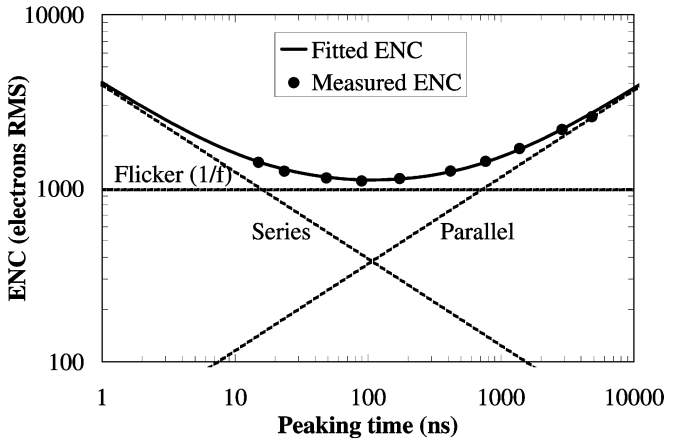

Fig. 6. ENC of the CSP connected to Hamamatsu APD (S8550) biased at 374 V.

The electronic timing resolution of the CSP connected to an Ortec 474 fast filter amplifier (20/20) and a leading edge discriminator (LED) Phillips 7404 is 0.56 ns (FWHM). The APD was biased at 374 V in order to have the proper noise figure. The coincidence timing resolution of this setup, with the LED replaced by an Ortec constant fraction discriminator (CFD) 934, against a BaF_2 scintillator and a photomultiplier tube (PMT), is 2.5 ns full-width at half-maximum (FWHM), using a ^{22}Na source and a 4×8 LSO array with pixel size of $2 \times 2 \times 5$ mm^3 coupled to the APD. An energy resolution of 17% (FWHM) has been measured. Further detailed results are presented in [5].

B. ICFSHB01 Measurements

The linearity of the CSP and third-order bipolar Gaussian shaper has been evaluated. Fig. 7 presents a measured curve of the output voltage as a function of the input charges. An average gain of 15.0 ± 0.3 mV/fC has been measured in the designed operating region (up to 130 k electrons), compared to 15.15 mV/fC in simulation.

The peaking time (1% to 99%) as a function of the input capacitance was evaluated. Table III compares the measured peaking time versus the simulations for input test capacitance of 0 and 12 pF.

The ENC of the analog front-end has been evaluated. In order to have an accurate estimate of charge gain (required to evaluate

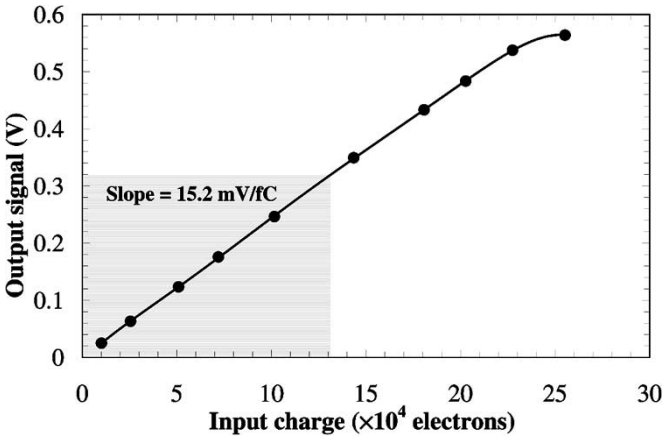

Fig. 7. Linearity of the analog front-end for an input test capacitance of 12 pF. A gain of 15.2 mV/fC as been fitted in the designed operating region (up to 130 k electrons).

TABLE III
COMPARISON OF THE MEASURED PEAKING TIME VERSUS SIMULATIONS

	Measurements	Simulations
0 pF	73.2±1.4 ns	74.0 ns
12 pF	80.4±1.8 ns	80.0 ns

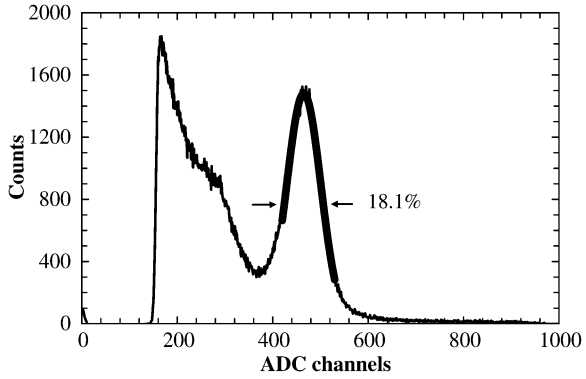

Fig. 8. Energy resolution of the analog front-end connected to one channel of the S8550 APD/LSO module for a ^{68}Ge source. The energy resolution is 18.1% FWHM.

the ENC), the injection capacitance of every channel has been measured on the test printed circuit board. An average minimum ENC of 902 $\pm$ 29 electrons rms was measured for an input test capacitance of 12 pF.

The energy resolution of the analog front-end was measured using a ^{68}Ge source and a 4×8 LSO array with pixel size of $2 \times 2 \times 5$ mm^3 coupled to the APD. The output of the shaper was fed into an Ortec 934 CFD. Fig. 8 presents the energy spectrum. The energy resolution is 18.1% (FWHM).

The electronic and coincidence timing resolution of the analog front-end were measured in order to validate our mathematical analysis. An Ortec 934 CFD was used, but without adding back the delayed signal into the CFD, as usually required to create a bipolar signal when using a unipolar shaper. Hence the CFD is then used as a ZCD, looking at the zero-cross of the bipolar signal of the integrated shaper. For the electronic timing resolution, the input pulse amplitude was set at the 511 keV photopeak level, representing a light output of 2300 ph-electron/MeV, and the APD gain was set at 50. The timing

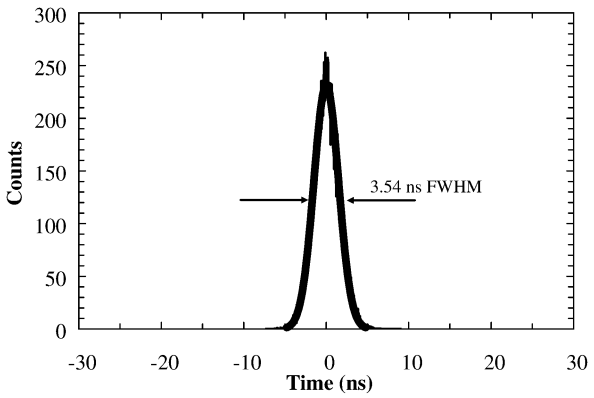

Fig. 9. Electronic timing resolution of the analog front-end using the CFD as a ZCD. A timing resolution of 3.54 ns FWHM was measured.

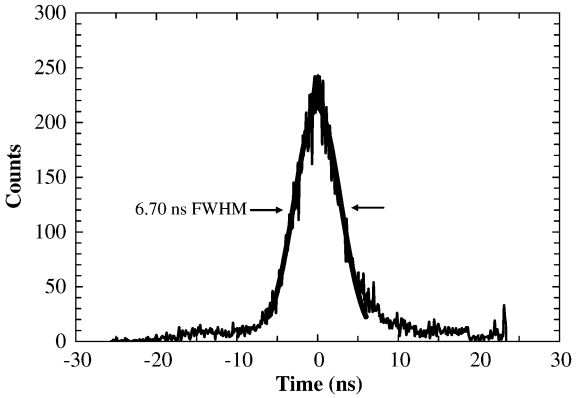

Fig. 10. Coincidence timing resolution of the analog front-end using the CFD as a ZCD with APD/LSO detector. A timing resolution of 6.70 ns FWHM was measured.

resolution obtained is 3.54 ns FWHM, as shown in Fig. 9. The coincidence timing resolution against a BaF_2 scintillator and a PMT was performed using a ^{68}Ge source. A timing resolution of 6.70 ns FWHM was obtained as shown in Fig. 10. The equivalent rms values are reported in Fig. 4.

IV. DISCUSSION

The measured ENC of the CSP was properly fitted mathematically, and an input-referred noise e_n of 0.9 nV/$\sqrt{(\text{Hz})}$ was obtained, which is in the same range as other CSPs used for PET imaging [9]–[11]. The difference between the ENC obtained with the CSP chip and the CSP-shaper chip could be explained by a smaller stray capacitance and differences in the electronic performance due to process variations. Originally, the preamplifier was optimized so that the minimum ENC would occur at a peaking time of 70 ns, and not at 100 ns as shown in Fig. 6. The explanation comes from an underestimation of the flicker noise coefficient. Preliminary results, from measurements on test devices that were included on the ICFSHLNA chip, show a KF_n about ten times higher than expected. Further investigations are under way to asses this issue. Even so, as the ENC varies slowly with the peaking time, this should not compromise the functionality of the analog front-end for our PET application.

The analog front-end exhibits excellent linearity in the operating region and even beyond. The measured peaking time fits accordingly with simulations.

Regarding the timing resolution, the mathematical model developed has been validated. From Fig. 4, one can see that the photoelectron statistics is limiting the timing resolution achievable. The next iteration will include on-chip timing discrimination and is expected to achieve equal or better resolution than in these measurements. A raising question is to identify an acceptable coincidence timing window, which would keep the number of random coincidences to an acceptable level, keeping in mind the power needed to achieve the required timing resolution.

V. Conclusion

The results obtained so far on the first two prototypes show good agreement with the simulations. The design respects the criteria of minimal power consumption, size, and mobility by minimizing the number of interconnections, making it suitable for a portable mobile PET scanner for rat studies. Further development to optimize the timing pickoff circuitry is planned.

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